IN THE DRAWINGS:

Please enter the replacement sheets for Figures 1 and 3 that are attached to this Amendment.

REMARKS

The Office Action of March 22, 2005 has been received and its contents carefully considered.

In response to the drawing objection in section 1 of the Office Action, the present Amendment forwards a replacement sheet of drawings in which Figure 1 is identified as prior art. Accordingly, the objection should be withdrawn.

In reply to the drawing objections in sections 2 and 3 of the Office Action, the present Amendment also forwards a replacement sheet for Figure 3. The replacement sheet illustrates a select transistor 69' and also schematically shows (with a dotted line) a wire 70' that connects the transistor 69' to the memory cell array region 50. As a result of these changes, the replacement sheet for Figure 3 shows a plurality of select transistors (69 and 69') that are arranged symmetrically with respect to the memory cell array 50. Accordingly, the objections in sections 2 and 3 of the Office Action should be withdrawn. It is noted that the specification has been amended to mention the new features 69' and 70' that are shown in the replacement sheet for Figure 3.

The present application is directed to the physical layout of a flash memory. It is important to distinguish between the layout of a circuit and the circuit itself (meaning electrical connections between components). Any particular circuit can be implemented by numerous possible layouts. For example, the circuit shown in Figure 1 of the present application's drawings has been implemented in the past using the prior art layout that is shown in Figure 2 of the application's drawings. However, the same circuit (Figure 1) can be implemented using the improved layout shown in Figure 3 of the application's drawings, thereby achieving the advantages noted in the application.

The Office Action rejects all of the claims for anticipation by Ichige et al (which will hereafter be called simply "Ichige"). In rejecting the claims, the Office Action draws attention to Ichige's Figures 24, 30, 39, and 41. Of these figures, only Figure 24 shows a physical layout.

The preambles of independent claims 1 and 3 specify "A layout of a flash memory having symmetric select transistors." The body of claim 1 recites a memory cell array and "polysilicon gates extending in a direction perpendicular to the memory cell array ...". Similarly, the body of independent claim 3 recites "polysilicon gates ... extending in a direction perpendicular to the memory cell array." It is respectfully submitted that these features are neither disclosed nor suggested by the reference. In particular, what is shown in Ichige's Figure 30, 39, and 41 are circuit diagrams. An ordinarily skilled person would appreciate that a circuit diagram only provides information about electrical connections. The lengths and directions of the wires shown in a circuit diagram, along with the placement in the diagram of the circuit components themselves, are selected for convenient illustration and have nothing to do with physical layout. As a result, it is respectfully submitted that Ichige's Figures 30, 39, and 40 would not have placed the inventions that are defined by independent claims 1 and 3 in the hands of an ordinarily skilled person. Nor would Ichige's circuit diagrams have provided an incentive for an ordinarily skilled person to select the layout recited in the independent claims.

Since the remaining two claims depend from the independent claims discussed above and recite additional limitations to further define the invention, they are patentable along with their independent claims and need not be further discussed.

AMENDMENT 6 10/643,876

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,

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